

Table of Contents

[Hardware vs. Software](#)

[Publications](#)

[Forum Posts](#)

[External Links](#)

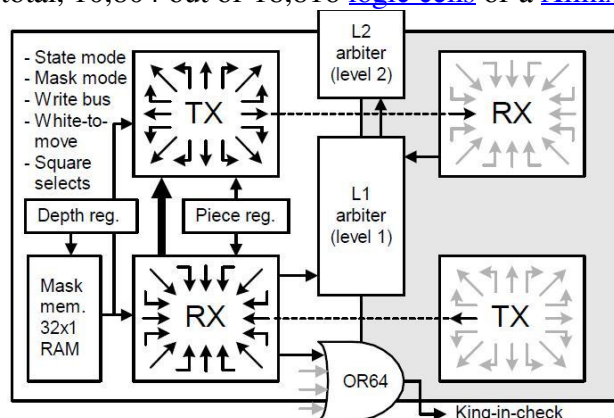
[References](#)

[What links here?](#)

[Home](#) * [Engines](#) * **MBChess**

MBChess,

a chess program by [Marc Boulé](#), written in [C](#). It was primarily used as test-bed for hardware based [FPGA move generation](#), which was subject of Boulé's Masters thesis in 2002 ^[1]. The FPGA approach performs a [Belle](#) like move generation method with find **victim** and find **aggressor** cycles in [MVV-LVA](#) manner. The move generator includes a [PCI](#) interface to connect it to the PC running MBChess. Communication is done via different commands, such as to instruct the move generator to [undo](#) the currently stored move, generate and return the next move and [execute](#) that move on its internal FPGA [board representation](#). In total, 10,804 out of 18,816 [logic cells](#) of a [Xilinx XCV800](#) ^[2] were used, 10,104 as [LUT](#), 700 as RAM ^[3].



A block diagram of a chess square with transmitter (TX) and the receiver (RX) ^[4]

Hardware vs. Software

MBChess is a very basic chess program, without [opening book](#), only rudimentary [evaluation](#), i.e. almost no

[king safety](#), and without [null move pruning](#). The reported ratings obtained on [FICS](#) are 1844 and 1692 for MBChess+FPGA and MBChess respectively ^[5]. Marc Boulé further concluded a bit disappointing results ^[6]. Even though the pure move generation speed is almost 5 times faster, when using full heuristics, this drops to about 2 times faster. He found that his FPGA move generator, can at best, make/unmake 10M moves a second, which due to PCI bus saturation, will not even transfer from FPGA to PC. [Crafty](#) could already make/unmake 30M moves a second on that machine, which implies the only way to speedup Crafty would be to make an FPGA with search and evaluation.

Publications

- [Marc Boulé](#) (2002). *An FPGA Move Generator for the Game of Chess*. Masters thesis, [McGill University](#), (Supervisor: [Zeljko Zilic](#), Co-Supervisor: [Monty Newborn](#)), [pdf](#)
- [Marc Boulé](#), [Zeljko Zilic](#) (2002). *An FPGA Move Generator for the Game of Chess*. [McGill University](#), [pdf](#)
- [Marc Boulé](#), [Zeljko Zilic](#) (2002). *An FPGA Move Generator for the Game of Chess*. [ICGA Journal](#), Vol. 25, No. 2, [pdf](#)

Forum Posts

- [A Response From Marc Boule](#) by [Slater Wold](#), [CCC](#), April 02, 2002
- [Re: Thesis by Marc Boule](#) by [Marc Boulé](#), [CCC](#), September 07, 2002
- [Re: Thesis by Marc Boule](#) by [Marc Boulé](#), [CCC](#), September 08, 2002

External Links

- [FICS Games Database - Statistics for mbchess](#)

References

1. [^] [Marc Boulé](#) (2002). *An FPGA Move Generator for the Game of Chess*. Masters thesis, [McGill University](#), (Supervisor: [Zeljko Zilic](#), Co-Supervisor: [Monty Newborn](#)), [pdf](#)
2. [^] [Re: Attention - Slater Wold](#) by [Marc Boulé](#), [CCC](#), April 10, 2003
3. [^] [Re: Thesis by Marc Boule](#) by [Marc Boulé](#), [CCC](#), September 08, 2002
4. [^] [Marc Boulé](#) (2002). *An FPGA Move Generator for the Game of Chess*. Masters thesis, [McGill University](#), (Supervisor: [Zeljko Zilic](#), Co-Supervisor: [Monty Newborn](#)), [pdf](#)
5. [^] [Marc Boulé](#), [Zeljko Zilic](#) (2002). *An FPGA Move Generator for the Game of Chess*. [ICGA Journal](#), Vol. 25, No. 2, pp. 8, [pdf](#)
6. [^] [A Response From Marc Boule](#) by [Slater Wold](#), [CCC](#), April 02, 2002

What links here?

Page

[Belle](#)

[Engines](#)

[FPGA](#)

[Marc Boulé](#)

[MBChess](#)

[McGill University](#)

[MVV-LVA](#)

Date Edited

Jan 18, 2018

Mar 10, 2018

Jul 9, 2016

Feb 17, 2015

Sep 29, 2012

Feb 12, 2018

Oct 26, 2017

[Up one Level](#)